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09/936,172	09/10/2001	Katsumi Adachi	OGOH:092	9751

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EXAMINER	
ABDULSELAM, ABBAS I	
ART UNIT	**PAPER NUMBER**
2674	6

DATE MAILED: 07/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/936,172	Applicant(s) ADACHI ET AL.	
	Examiner Abbas I Abdulselam	Art Unit 2674	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 January 0102*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *102* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *See Continuation Sheet* is/are allowed.

6)☒ Claim(s) *2,3,6,18,19,70,71 and 74* is/are rejected.

7)☒ Claim(s) *See Continuation Sheet* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3, 5*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Continuation of Disposition of Claims: Claims allowed are 1,4,5,7,10-12,15-17,20-23,26-28,31-33,36-39,42-45,48-51,54-57,60-63,66-69,72,73,75,78-80,83-85,88,89,91,94,95,97,100 and 101.

Continuation of Disposition of Claims: Claims objected to are 8,9,13,14,24,25,29,30,34,35,40,41,46,47,52,53,58,59,64,65,76,77,81,82,86,87,90,92,93,96,98,99 and 102.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2-3 6, 18-19, 70, 71 and 74 rejected under 35 U.S.C. 103(a) as being unpatentable over Troutman (USPN 6157356) in view of Asari et al. (USPN 5644329).

Regarding claims 2-3, 6, 18-19, 70, 71 and 74, Troutman teaches that a Gray-scale operation of the display in terms of dividing the frame time T.sub.f into multiple sub-frames T.sub.sfk and addressing all row lines during each sub-frame time. Troutman discloses that each column line is either V.sub.h or V.sub.l during the line time, and this voltage is written into the storage capacitor (104) of all pixels along the activated row line. Troutman also teaches that for n bits of gray scale, there are n sub-frames, and the sum of all sub-frame times equals the frame time T.sub.f. Troutman discloses that a pixel's luminance which is proportional to the sub-frame time, and each of the sub-frame times is weighted to produce the 2.sup.n gray scale levels. (Col. 3, lines 23-33). Furthermore, Troutman discloses a display with M rows and N columns, each sub-frame requiring M.times.N bits of data, and these are stored in a buffer memory. Troutman indicates the time required to transfer all M.times.N bits is the write time T.sub.w, and this time must be less than the sub-frame time for the least significant bit. (col. 3, lines 23-33).

Troutman doest not teach "simultaneously with outputting a signal having a value of a signal level via each of signal lines, the value of the signal level being selected from values of a

plurality of signal levels in accordance with digital image data and the number of the plurality of signal levels being fewer than the number of display gray scales".

Asari et al. (USPN 5644329) on the other teaches during a selection time, an L number of signals developed on the time axis are applied to row electrodes as shown in formula (5). Asari teaches that when a liquid crystal display element is driven, the L number of signals re dispersed in one frame and applied to row electrodes whereby a relaxation phenomenon of liquid crystal can be suppressed. Asari illustrates a reduction of the contrast ratio of a liquid crystal display element, which can be suppressed by dispersing the L number of signals in one frame and applying the signals. See col. 11, lines 8-25, Fig. 2 and formula (5).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Troutman's display system to adapt Asari's number of signals, L as expressed in formula 5 (col. 4, line 50). One would have been motivated in view of the suggestion in Asari that that manipulating L with respect to expression (5) would provide the desired signal value and the number of signal levels. The use of signal value determination helps form an appropriate data signal in a display system as taught by Asari.

Allowable Subject Matter

2. Claims 8-9, 13-14, 24-25, 29-30, 34-35, 40-41, 46-47, 52-53, 58-59, 64-65, 76-77, 81-82, 86-87, 90, 92-93, 96, 98-99 and 102 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

3. Claims 1, 4-5, 7, 10-12, 15-17, 20-23, 26-28, 31-33, 36-39, 42-45, 48-51, 54-57, 60-63, 66-69, 72-73, 75, 78-80, 83-85, 88-89, 91, 94-95, 97 and 100-101 are allowed.

Regarding claim 1, prior art does not teach A method of driving an active matrix display device wherein one frame comprises a plurality of sub-frames each comprising a write time and a hold time and a gray scale display is brought about by the cumulative effect of the hold times the method comprising the steps of: simultaneously with outputting a signal having a value of a signal level via each of signal lines, the value of the signal level being selected from values of a plurality of signal levels in accordance with digital image data and the number of the plurality of signal levels being fewer than the number of display gray scales, randomly scanning scan lines other than one predetermined scan line in a predetermined sequence in the hold time of each of the sub-frames corresponding to the one predetermined scan line so that any one sub-frame is not written to any one scan line more than once wherein one frame period is such that in each respective scan line, the writing of each of the plurality of sub-frames is substantially brought about and the hold time of each of the sub-frames is ensured to bring about gray scale display driving.

Regarding claim 4, prior art does not teach a method of driving an active matrix display device wherein one frame comprises a plurality of sub-frames each comprising a write time and a hold time and a gray scale display is brought about by the cumulative effect of the hold times, the method comprising the steps of: simultaneously with outputting a signal having a value of a signal level via each of signal lines, the value of the signal level being selected from values of a

plurality of signal levels in accordance with digital image data and the number of the plurality of signal levels being fewer than the number of display gray scales, driving the display device such that the period of the frame is set to NH[1+K(2''' -1)]=NHL where N is the number of sub-frames, H is a horizontal scanning period, 1:2:4:...:2N-1 is the weightings of the hold times, L is the number of scan lines, and K is a positive integer.

Regarding claim 5, prior art does not teach a method of driving an active matrix display device wherein one frame comprises a plurality of sub-frames each comprising a write time and a hold time and a gray scale display is brought about by the cumulative effect of the hold times, the method comprising the steps of: simultaneously with outputting a signal having a value of a signal level via each of signal lines, the value of the signal level being selected from values of a plurality of signal levels in accordance with digital image data and the number of the plurality of signal levels being fewer than the number of display gray scales, driving the display device such that the period of the frame is set to NH[1- FK(i)] = NHL where N is the number of sub-frames, H is a horizontal scanning period, KW is the weighting of the hold time of the period of an ith sub-frame where i=1,2,..., N, and L is the number of scan lines.

Regarding claim 17, prior art does not teach an active matrix display device including a first substrate and a second substrate confronting the first substrate with a liquid crystal layer there between, the first substrate having formed thereon switching elements corresponding to the intersection points of a plurality of signal lines and a Plurality of scan lines arranged in a matrix, pixel electrodes connected to the switching elements, and storage capacitors connected to the

pixel electrodes and the second substrate having formed thereon a counter electrode, wherein one frame comprises a plurality of sub-frames each comprising a write time and a hold time and a gray scale display is brought about by the cumulative effect of the hold times, the display device comprising a signal line driver circuit for selecting a value of a voltage level from values of a plurality of voltage levels in accordance with digital image data and outputting a voltage having the selected value via each of the signal lines, the number of the plurality of voltage levels being fewer than the number of display gray scales and a scan line driver circuit for randomly scanning the plurality of scan lines by scanning scan lines other than one predetermined scan line in a predetermined sequence in the hold time of each of the sub-frames corresponding to the one predetermined scan so that any one sub-frame is not written to any one scan line more than once wherein one frame period is such that in each respective scan line, the writing of each of the plurality of sub-frames is substantially brought about and the hold time of each of the sub-frames is ensured to bring about gray scale display driving.

Regarding claim 20, prior art does not teach an active matrix display device including a first substrate and a second substrate confronting the first substrate with a liquid crystal layer there between, the first substrate having formed thereon switching elements corresponding to the intersection points of a plurality of signal lines and a plurality of scan lines arranged in a matrix, pixel electrodes connected to the switching elements, and storage capacitors connected to the pixel electrodes and the second substrate having formed thereon a counter electrode, wherein one frame comprises a plurality of sub-frames each comprising a write time and a hold time and a gray scale display is brought about by the cumulative effect of the hold times, the display device

comprising: a signal line driver circuit for selecting a value of a voltage level from values of a plurality of voltage levels in accordance with digital image data and outputting a voltage having the selected value via each of the signal lines, the number of the plurality of voltage levels being fewer than the number of display gray scales and a scan line driver circuit for selecting the scan lines so that the period of the frame is NH[1+K(2N -1)]=NHL where N is the number of sub-frames, H is a horizontal scanning period, 1:2:4:...:2N-1 is the weightings of the hold times, L is the number of scan lines, and K is a positive integer.

Regarding claim 21, prior art does not teach an active matrix display device including a first substrate and a second substrate confronting the first substrate with a liquid crystal layer there between, the first substrate having formed thereon switching elements corresponding to the intersection points of a plurality of signal lines and a plurality of scan lines arranged in a matrix, pixel electrodes connected to the switching elements, and storage capacitors connected to the pixel electrodes and the second substrate having formed thereon a counter electrode, wherein one frame comprises a plurality of sub-frames each comprising a write time and a hold time and a gray scale display is brought about by the cumulative effect of the hold times, the display device comprising: a signal line driver circuit for selecting a value of a voltage level from values of a plurality of voltage levels in accordance with digital image data and outputting a voltage having the selected value via each of the signal lines, the number of the plurality of voltage levels being fewer than the number of display gray scales and a scan line driver circuit for selecting the scan lines so that the period of the frame is NH[1- EK(i)] = NH where N is the number of sub-frames,

H is a horizontal scanning period, K(i) is the weighting of the hold time of the period of an ith sub-frame where i=1,2,..., N, and L is the number of scan lines.

Regarding claim 22, the prior art does not teach an active matrix display device including a first substrate and a second substrate confronting the first substrate with a liquid crystal layer there between, the first substrate having formed thereon switching elements corresponding to the intersection points of a plurality of signal lines and a plurality of scan lines arranged in a matrix, pixel electrodes connected to the switching elements, and storage capacitors connected to the pixel electrodes and the second substrate having formed thereon a counter electrode, wherein one frame comprises a plurality of sub-frames each comprising a write time and a hold time and a gray scale display is brought about by the cumulative effect of the hold times, the display device comprising: a signal line driver circuit for selecting a value of a voltage level from values of a plurality of voltage levels in accordance with digital image data and outputting a voltage having the selected value via each of the signal lines, the number of the plurality of voltage levels being at least three and fewer than the number of display gray scales and the selection being carried out so that the degree of freedom of the voltage levels usable for one gray scale within the period of the one frame is two; and a scan line driver circuit for sequentially scanning or randomly scanning the scan lines.

Regarding claim 69, prior art does not teach active matrix display device including a first substrate and a second substrate confronting the first substrate with a luminescent layer there between, the first substrate having formed thereon first switching elements corresponding to the

intersection points of a plurality of signal lines and a plurality of scan lines arranged in a matrix, second switching elements connected to the first switching elements, pixel electrodes connected to the second switching elements, and power supply lines connected to a side of the second switching elements differing from that to which the pixel electrodes are connected and the second substrate having formed thereon a counter electrode, wherein one frame comprises a plurality of sub-frames each comprising a write time and a hold time and a gray scale display is brought about by the cumulative effect of the hold times, the display device comprising: a signal line driver circuit for selecting a value of a voltage level from values of a plurality of voltage levels in accordance with digital image data and outputting a voltage having the selected value via each of the signal lines, the number of the plurality of voltage - levels being fewer than the number of display gray scales and a scan line driver circuit for randomly scanning the plurality of scan lines by scanning scan lines other than one predetermined scan - line in a predetermined sequence in the hold time of each of the sub-frames corresponding to the one predetermined scan so that any one sub-frame is not written to any one scan line more than once wherein one frame period is such that in each respective scan line, the writing of each of the plurality of sub-frames is substantially brought about and the hold time of each of the sub-frames is ensured to bring about gray scale display driving.

Regarding claim 72, prior art does not teach an active matrix display device including a first substrate and a second substrate confronting the first substrate with a luminescent layer there between, the first substrate having formed thereon first switching elements corresponding to the intersection points of a plurality of signal lines and a plurality of scan lines arranged in a matrix,

second switching elements connected to the first switching elements, pixel electrodes connected to the second switching elements, and power supply lines elements connected to the first switching elements, pixel electrodes connected to the second switching elements, and power supply lines connected to a side of the second switching elements differing from that to which the pixel electrodes are connected and the second substrate having formed thereon a counter electrode, wherein one frame comprises a plurality of sub-frames SF1, SF2, ..., SFn, where n is a natural number, each comprising a write time and a hold time and a gray scale display is brought about by the cumulative effect of the hold times, the display device comprising a signal line driver circuit for selecting a value of a voltage level from values of a plurality of voltage levels in accordance with digital image data and outputting a voltage having the selected value via each of the signal lines, the number of the plurality of voltage levels being fewer than the number of display gray scales; and a scan line driver circuit for selecting the scan lines so that a selection sequence of the periods of the sub-frames is repeated cyclically as in SF1-> SF2--> ...--~ SFn--> SF1--j SF2--> ...-* SFn.

Regarding claim 73, prior art does not teach an active matrix display device including a first substrate and a second substrate confronting the first substrate with a luminescent layer there between, the first substrate having formed thereon first switching elements corresponding to the intersection points of a plurality of signal lines and a plurality of scan lines arranged in a matrix, second switching elements connected to the first switching elements, pixel electrodes connected to the second switching elements, and power supply lines connected to a side of the second switching elements differing from that to which the pixel electrodes are connected and the

second substrate having formed thereon a counter electrode, wherein one frame comprises a plurality of sub-frames each comprising a write time and a hold time and a gray scale display is brought about by the cumulative effect of the hold times, the display device comprising: a signal line driver circuit for selecting a value of a voltage level from values of a plurality of voltage levels in accordance with digital image data and outputting a voltage having the selected value via each of the signal lines, the number of the plurality of voltage levels being fewer than the number of display gray scales and a scan line driver circuit for selecting the scan lines so that the period of the frame is NH[1- EK(i)] = NHL where N is the number of sub-frames, H is a horizontal scanning period, K(i) is the weighting of the hold time of the period of an ith sub-frame where i=1,2,..., N, and L is the number of scan lines.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following art is cited for further reference.

U.S. Pat. No. 6,570,550 to Handschy et al.

5. Any inquiry concerning this communication or earlier communication from the examiner should be directed to Abbas Abdulselam whose telephone number is (703) 305-8591. The examiner can normally be reached on Monday through Friday (9:00-5:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Hjerpe, can be reached at (703) 305-4709.

Any response to this action should be mailed to:

Commissioner of patents and Trademarks

Washington, D.C. 20231 or faxed to:

(703) 872-9314

Hand delivered responses should be brought to Crystal Park II, Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology center 2600 customer Service office whose telephone number is (703) 306-0377.

Abbas Abdulselam

Examiner

Art Unit 2674

July 15, 2004

XIAO WU
PRIMARY EXAMINER